

FIG. 1

FIG. 2 is a block diagram of a network architecture for ATM signaling interception.

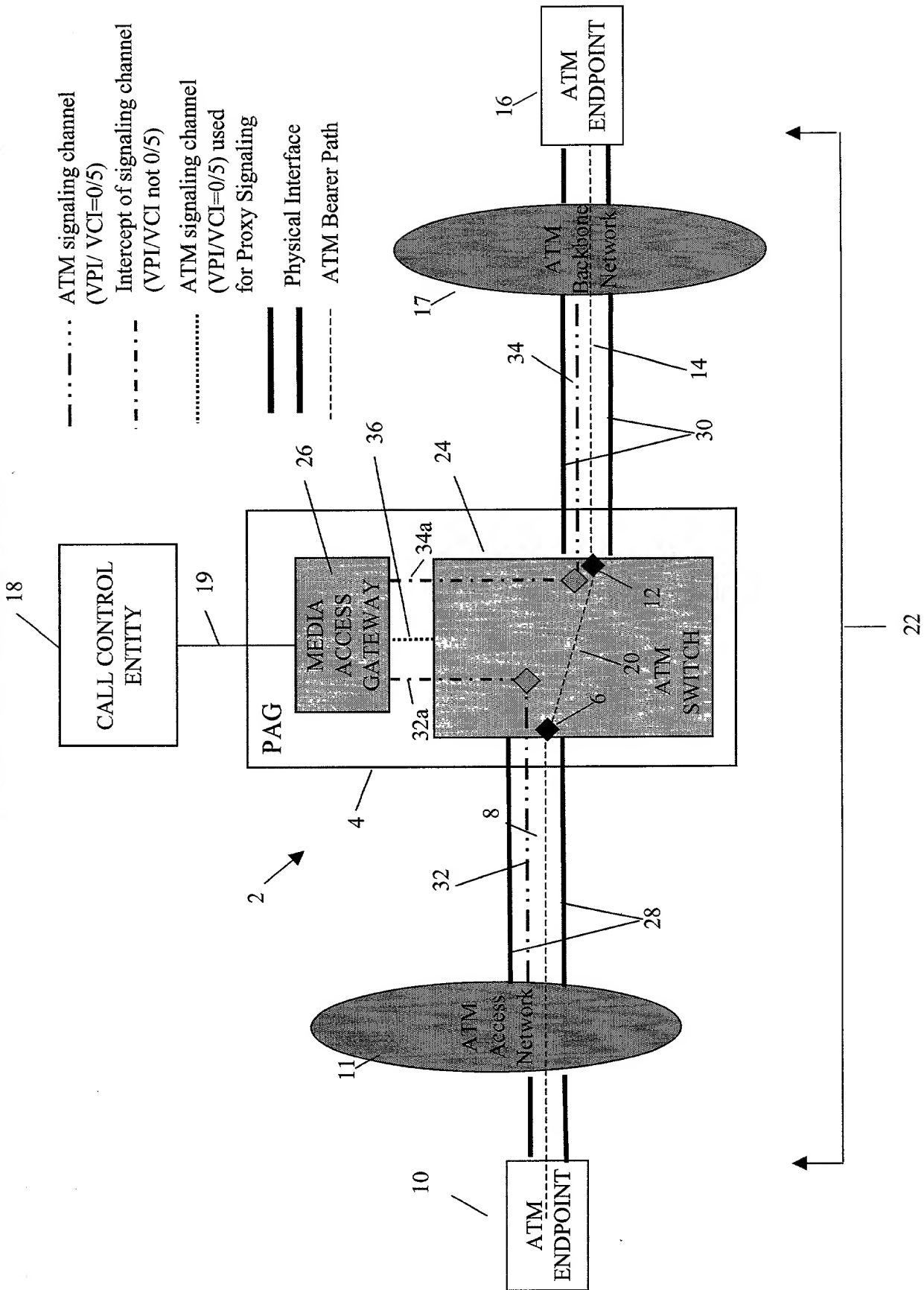


FIG. 2

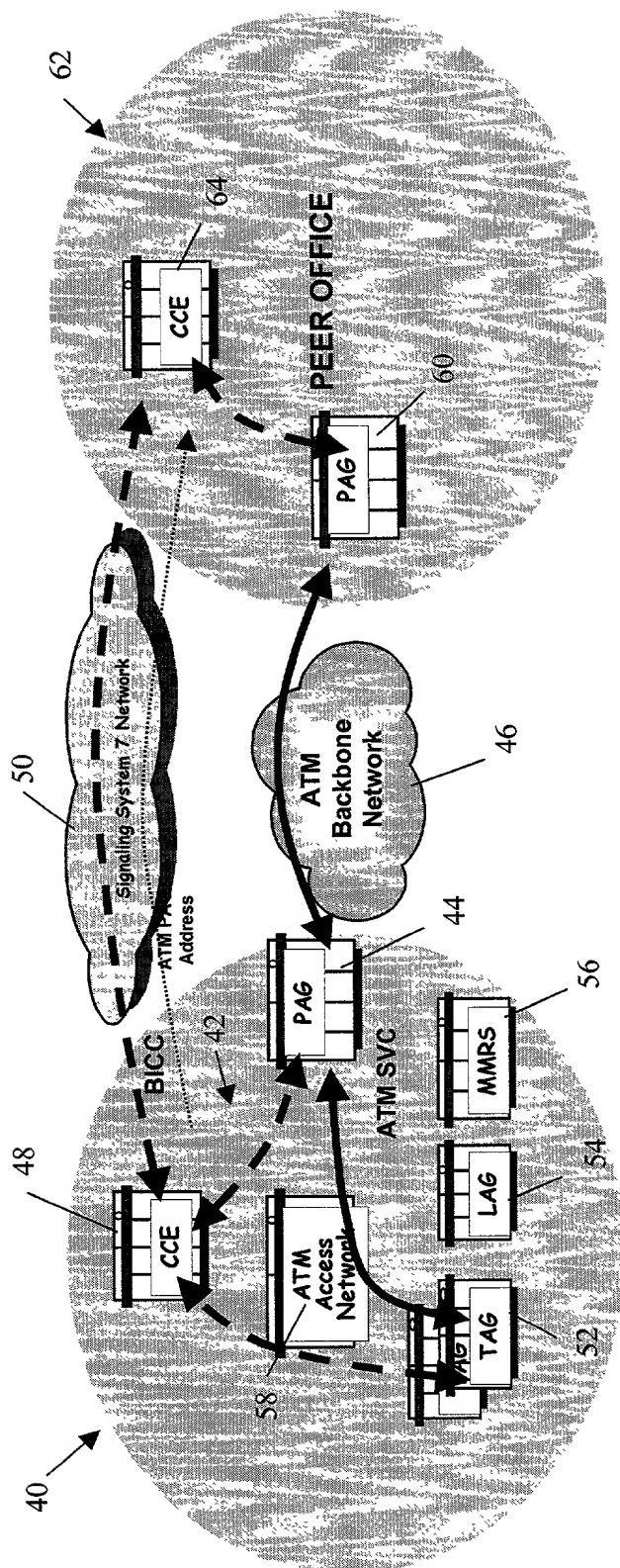


FIG. 3

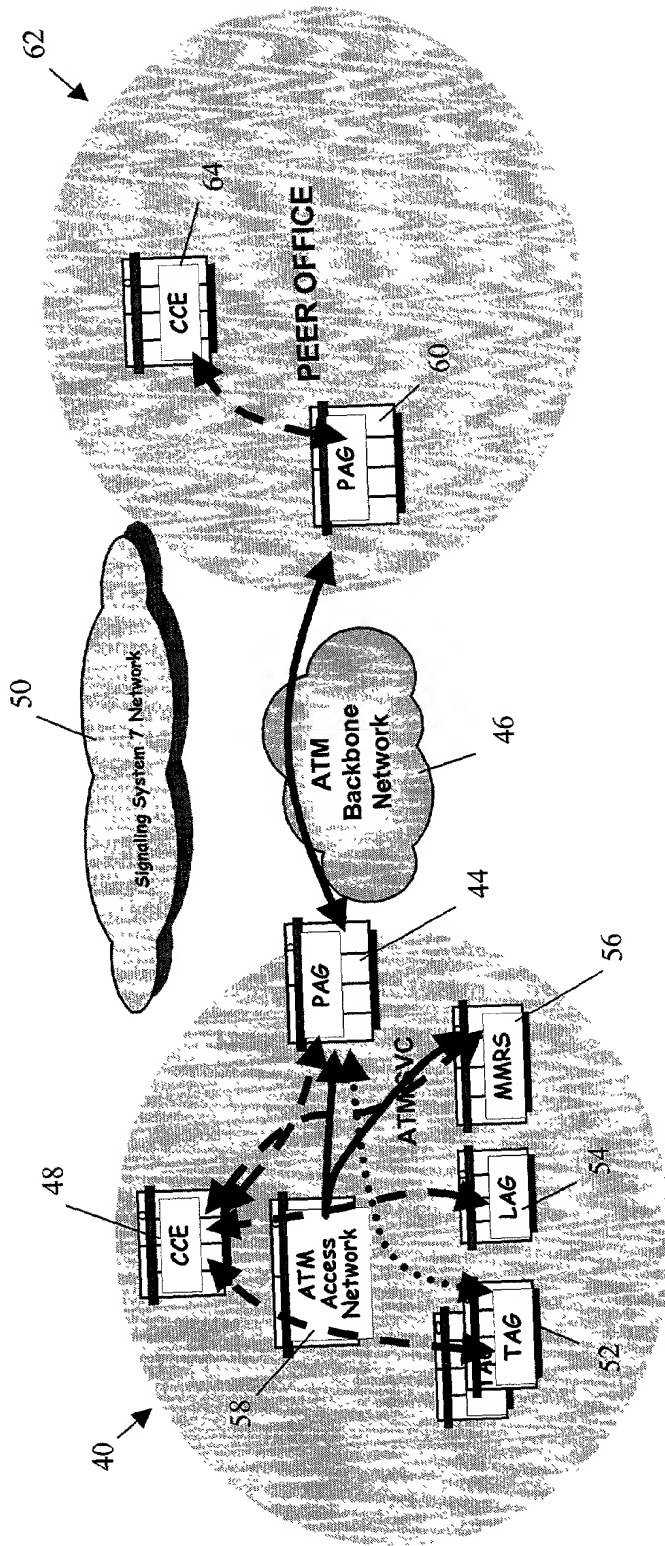


FIG. 4

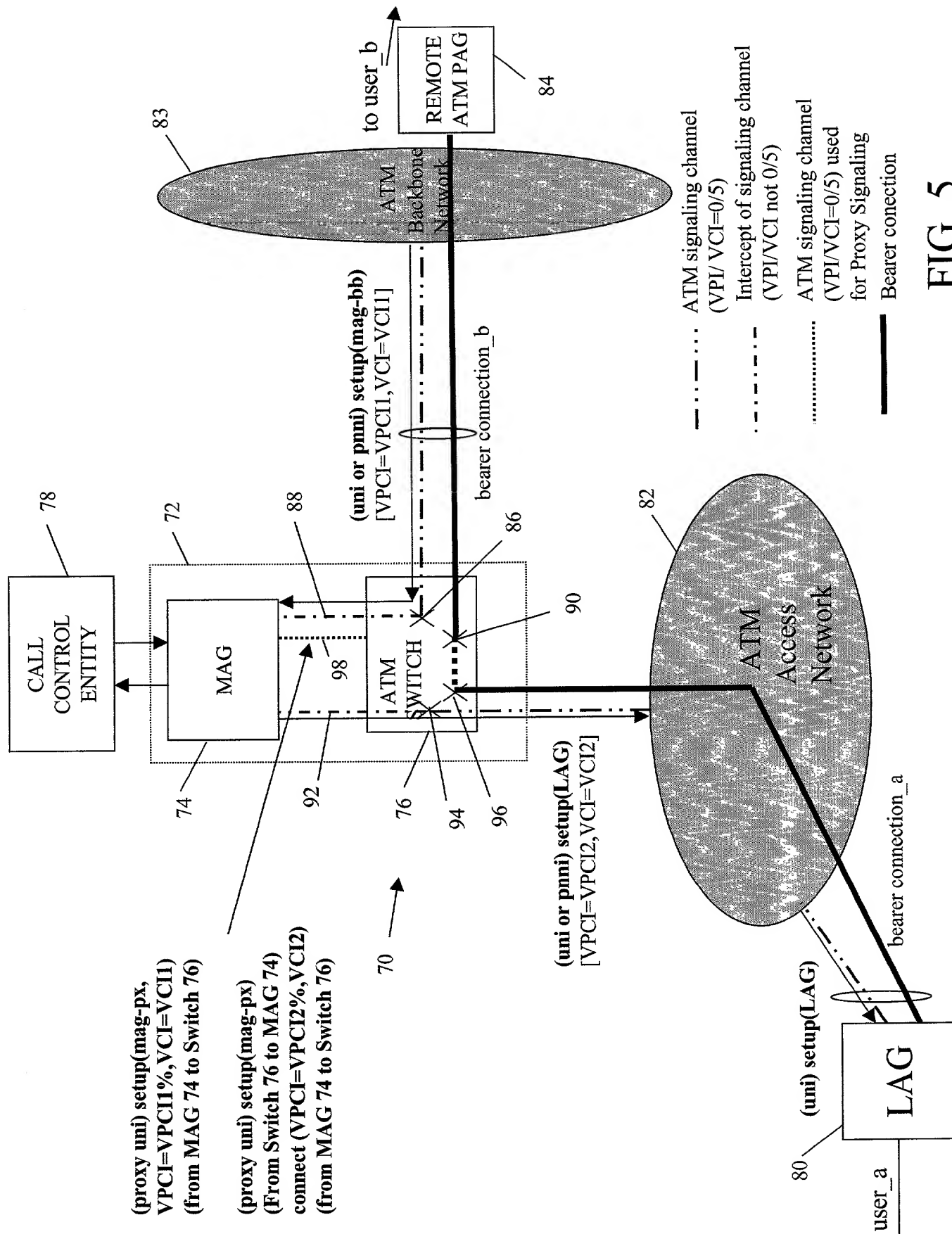


FIG. 5

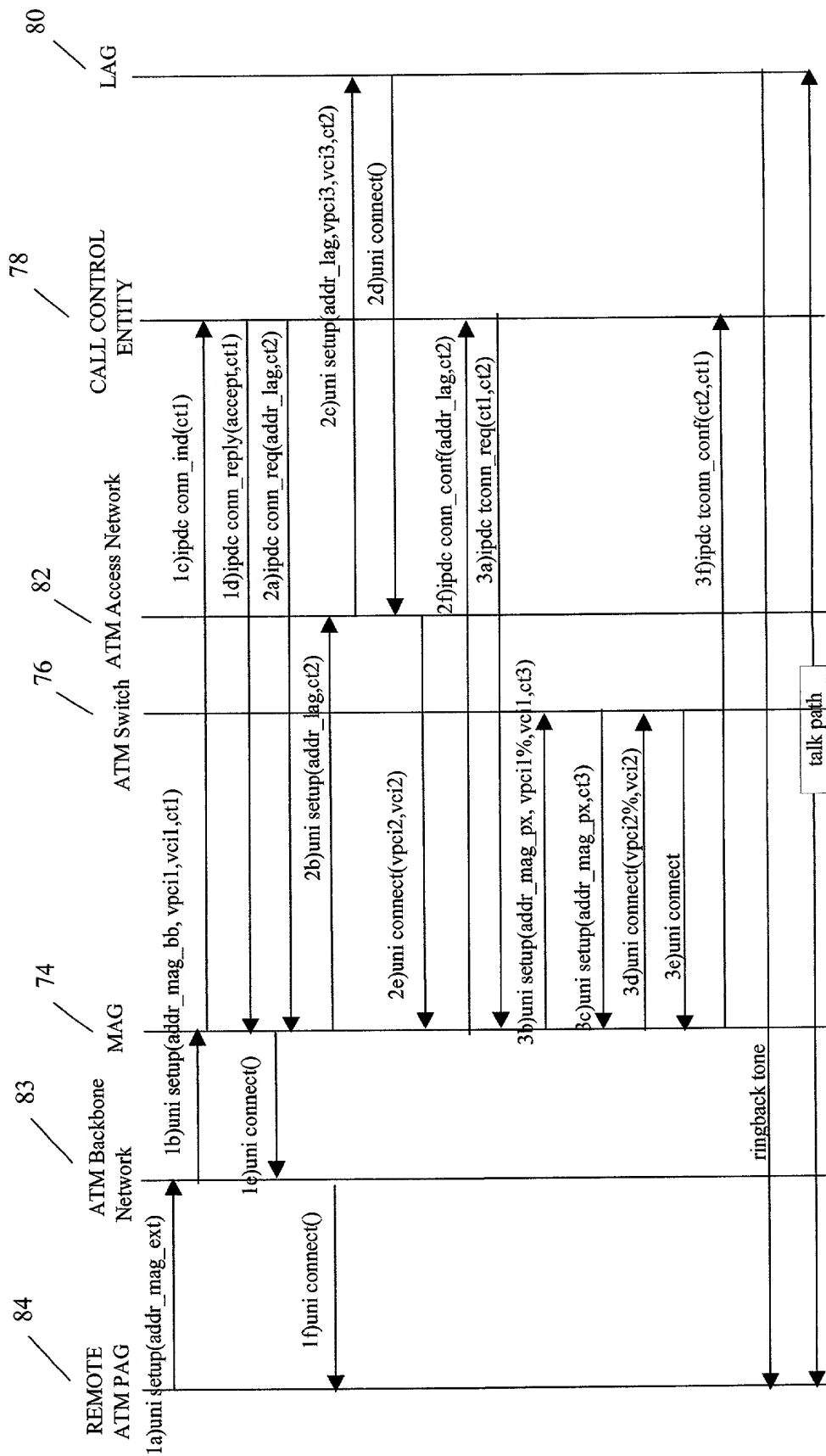


FIG. 6